Amendments to the Claims:

Please amend claims 1, 7, 14, and 21. Following is a complete listing of the claims pending in the application, as amended:

1. (Currently Amended) A phase adjusting circuit for generating a phase adjusting value based on the phase difference of a target clock signal and an input signal, the phase adjusting circuit comprising:

a phase-frequency detector ~~for generating~~ configured to generate a first control signal and a second control signal by comparing the phase of the input signal with the phase of the target clock signal;

a clock generator ~~for generating~~ configured to generate a reference clock;

a counter connected to the phase-frequency detector and the ~~counter~~clock generator and ~~for generating~~ configured to generate a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal, and ~~generating~~ to generate a second counting value by counting the number of cycles of the reference clock during the duration of the second control signal; and

a decision logic circuit connected to the counter and configured to:

~~for generating~~ generate a third counting value based on the first counting value and the second counting value,

~~calculating~~ calculate the sum of a plurality of the third counting values,

if the number of the plurality of the third counting values is greater than a predetermined number of cycles, provide the phase adjusting value,

wherein the phase adjusting value is set ~~setting the phase adjusting value~~ to zero if the sum is within a specified range, and is set

based on ~~setting the phase adjusting value according to the~~ sum if the sum is outside the specified range.

2. (Currently Amended) The phase adjusting circuit of claim 1, wherein the first control signal is generated ~~when~~if the phase of the input signal leads the phase of the target clock signal.

3. (Currently Amended) The phase adjusting circuit of claim 1, wherein the second control signal is generated ~~when~~if the phase of the input signal lags the phase of the target clock signal.

4. (Previously Presented) The phase adjusting circuit of claim 1, wherein the reference clock frequency is N times the frequency of the target clock signal and the specified range ranges from a positive number of N/2 to a negative number having an absolute value of N/2.

5. (Original) The phase adjusting circuit of claim 1, wherein the first counting value is a positive value, the second counting value is a negative value, and the third counting value is the sum of the first counting value and the second counting value.

6. (Original) The phase adjusting circuit of claim 1, wherein the phase-frequency detector is further able to receive a protection signal to stop outputting the phase adjusting value for avoiding interference generated from an unstable input signal.

7. (Currently Amended) A clock signal adjusting circuit comprising:

a phase adjusting circuit for generating a phase adjusting value based on an input signal and a target clock signal, the phase adjusting circuit comprising:

a phase-frequency detector ~~for generating~~ configured to generate a first control signal and a second control signal by comparing the phase of the input signal with the phase of the target clock signal;

a clock generator ~~for generating~~ configured to generate a second reference clock;

a counter connected to the phase-frequency detector and the clock generator ~~for generating~~ configured to generate a first counting value by counting the number of cycles of the second reference clock during the duration of the first control signal, and ~~generating~~ to generate a second counting value by counting the number of cycles of the second reference clock during the duration of the second control signal; and

a decision logic circuit connected to the counter and configured to:

~~for generating~~ generate a third counting value based on the first counting value and the second counting value,

~~calculating~~ calculate the sum of a plurality of the third counting values,

if the number of the plurality of the third counting values is greater than a predetermined number of cycles, provide the phase adjusting value,

wherein the phase adjusting value is set ~~setting the phase adjusting value~~ to zero if the sum is within a specified range, and is set based on ~~setting the phase adjusting value according to~~ the sum if the sum is outside the specified range; and

a frequency divider connected to the phase adjusting circuit for adjusting the target clock signal by dividing the frequency of a first reference clock based on the phase adjusting value.

8. (Cancelled)

9. (Currently Amended) The clock signal adjusting circuit of claim 7, wherein the first control signal is generated ~~when~~if the phase of the input signal leads the phase of the target clock signal.

10. (Currently Amended) The clock signal adjusting circuit of claim 7, wherein the second control signal is generated ~~when~~if the phase of the input signal lags the phase of the target clock signal.

11. (Previously Presented) The clock signal adjusting circuit of claim 7, wherein the second reference clock frequency is N times the frequency of the target clock signal and the specified range ranges from a positive number of N/2 to a negative number having an absolute value of N/2.

12. (Currently Amended) The clock signal adjusting circuit of claim 7, wherein the frequency divider comprises:

a counter for counting the cycle number of cycles of the first reference clock and resetting the cycle number after a specified number of cycles of the first reference clock;

a register for storing the phase adjusting value;

a comparator connected to the counter and the register for generating an enable signal ~~when~~if the cycle number of the first reference clock is equal to the phase adjusting value;

a pulse generator connected to the comparator for generating an impulse ~~when~~if receiving the enable signal;

a flip-flop having a trigger input terminal connected to the pulse generator for outputting the target clock signal while receiving the impulse; and

an inverter having an input terminal for receiving the target clock signal and inverting the target clock signal to feedback to the input of the flip-flop.

13. (Original) The clock signal adjusting circuit of claim 7 being applied to an optical disc drive, the input signal being a wobble signal of an optical disc, the target clock signal being a corresponding wobble clock generated by the optical disc drive based on the wobble signal.

14. (Currently Amended) A method for adjusting clock signal comprising:

generating a first control signal and a second control signal by comparing the phase of an input signal with the phase of a target clock signal;

generating a first counting value by counting the number of cycles of a second reference clock during the duration of the first control signal;

generating a second counting value by counting the number of cycles of the second reference clock during the duration of the second control signal;

generating a third counting value based on the first counting value and the second counting value;

calculating the sum of a plurality of the third counting values;

if the number of the plurality of the third counting values is greater than a predetermined number of cycles, setting a phase adjusting value, wherein the phase adjusting value is set to zero if the sum is within a specified range and ~~setting~~ the phase adjusting value is set based on ~~according to~~ the sum if the sum is outside the specified range; and

adjusting the target clock signal by dividing the frequency of a first reference clock based on the phase adjusting value.

15. (Cancelled)

16. (Currently Amended) The method of claim 14, wherein the first control signal is generated ~~when~~if the phase of the input signal leads the phase of the target clock signal.

17. (Currently Amended) The method of claim 14, wherein the second control signal is generated ~~when~~if the phase of the input signal lags the phase of the target clock signal.

18. (Previously Presented) The method of claim 14, wherein the the second reference clock frequency is N times the frequency of the target clock signal and the specified range ranges from a positive number of N/2 to a negative number having an absolute value of N/2.

19. (Currently Amended) The method of claim 14 further comprising:

counting the cycle number of cycles of the first reference clock and resetting the cycle number after each predetermined number of cycles of the first reference clock;

generating an enable signal ~~when~~if the cycle number of the first reference clock is equal to the phase adjusting value;

generating an impulse when receiving the enable signal;

outputting the target clock signal while receiving the impulse; and

inverting the target clock signal to feedback to the input.

20. (Original) The method of claim 14 being applied to an optical disc drive, the input signal being a wobble signal of an optical disc, the target clock signal being a corresponding wobble clock generated by the optical disc drive based on the wobble signal.

21. (Currently Amended) An apparatus for adjusting a clock signal comprising:

means for generating a first control signal and a second control signal by comparing the phase of an input signal with the phase of a target clock signal;

means for generating a first counting value by counting the number of cycles of a second reference clock during the duration of the first control signal;

means for generating a second counting value by counting the number of cycles of the second reference clock during the duration of the second control signal;

means for generating a third counting value based on the first counting value and the second counting value;

means for calculating the sum of a plurality of the third counting values;

means for setting a phase adjusting value if the number of the plurality of the third counting values is greater than a predetermined number of cycles, wherein the phase adjusting value is set to zero if the sum is within a specified range and ~~setting~~ the phase adjusting value is set based on ~~according to~~ the sum if the sum is outside the specified range; and

means for adjusting the target clock signal by dividing the frequency of a first reference clock based on the phase adjusting value.

22. (Currently Amended) The apparatus of claim 21, wherein the first control signal is generated ~~when~~if the phase of the input signal leads the phase of the target clock signal.

23. (Currently Amended) The apparatus of claim 21, wherein the second control signal is generated ~~when~~if the phase of the input signal lags the phase of the target clock signal.

24. (Previously Presented) The apparatus of claim 21, wherein the second reference clock frequency is N times the frequency of the target clock signal and the specified range ranges from a positive number of N/2 to a negative number having an absolute value of N/2.

25. (Currently Amended) The apparatus of claim 21 further comprising:

means for counting the cycle number of cycles of the first reference clock and resetting the cycle number after each N cycles of the first reference clock;

means for generating an enable signal ~~when~~if the cycle number of the first reference clock is equal to the phase adjusting value;

means for generating an impulse when receiving the enable signal;

means for outputting the target clock signal while receiving the impulse; and

means for inverting the target clock signal to feedback to the input.

26. (Previously Presented) The apparatus of claim 21 being applied to an optical disc drive, the input signal being a wobble signal of an optical disc, the target clock signal being a corresponding wobble clock generated by the optical disc drive based on the wobble signal.